ADDRESSABLE IMAGER WITH REAL TIME DEFECT DETECTION AND SUBSTITUTION

Cross-Reference to Related Applications

[0001] This application claims the benefit of U.S. Provisional Application No. 60/267,005, filed February 7, 2001, the contents of which are incorporated herein by reference.

Field of the Invention

[0002] The present invention is directed to an x-y addressable video imaging system with real time defect detection and substitution, and, more particularly to such an imaging system in which the imager and the defect detection and correction circuits are on the same substrate.

Background of the Invention

[0003] Defects in the individual picture element (pixel) cells that constitute a video imager, unless corrected, may cause defects in the output images produced by the imager. These defects may appear as bright spots or lines in an otherwise dark image or dark spots or lines in an otherwise bright image. Because video imagers typically include a large number of pixel cells, it is difficult to produce imagers that are free of such defects.

[0004] One way of effectively increasing the yield of imagers is to substitute a corrected signal component for that produced by any individual defective element of an imager. However, before such a correction can take place, it is necessary to detect those elements of the imager which are defective.

[0005] One proposed solution to this problem involves (1) analyzing the output signal from an imager, in the absence of an image, to detect the location of each then-existing defective element, (2) permanently storing the location of each defective element in a memory which is associated with the imager, and (3) during subsequent use of the imager, substituting a corrected signal for the signal produced by each detective element as determined by its location stored in the memory. This proposed solution may be impractical because many defects are

temperature dependent. Therefore, defective elements present during subsequent use of the imager may not have been present at the time of analysis and storage of the location of defective elements in the memory. In any case, the requirement for a memory associated with the imager increases the cost of a solid-state television camera employing this proposed solution to the problem of detective imager elements.

[0006] Many systems exist which detect defective pixels in an imager array with reference to a test pattern or other fixed image. For examples, dark current defects in an imager may be detected by analyzing the image obtained when the camera's lens is capped. Similarly, defects that cause dark pixels may be detected by imaging a flat white test card. Errors detected by these methods must be stored so that they may be corrected when the camera captures active video images.

[0007] United States Patent No. 4,253,120 to Peter A. Levine, entitled DEFECT DETECTION MEANS FOR CHARGE TRANSFER IMAGER, describes circuitry for determining and correcting defects in the pixels of an x-y imager using active video data. In the system described by this patent, a low-resolving power optical element is used to focus an image onto an imager that has a higher resolution than the resolving power of the optics. The difference between the resolution of the imager and the resolving power of the lens is used to distinguish errors in the imager array from transitions in the image. The referenced patent describes a charge-coupled device (CCD) imager array, which is formed on one substrate, and a correction circuit, which is formed on a separate substrate. Because the imager and the correction circuit are on separate substrates, the device is difficult to make, requiring two integrated circuit fabrications, and is relatively large in size.

Summary of the Invention

[0008] The present invention is embodied in a video imaging system formed on a single substrate, the video imaging system includes an imaging array having a plurality of picture elements (pixels). Each pixel is adapted to receive light and convert the light to an electrical signal. An analog to digital converter formed in said substrate converts the electrical signals from the pixels into digital pixel signals and a first circuit formed in said substrate analyzes the pixel signals to provide a defective pixel output signal indicating, as the digital pixel signal

corresponding to the pixels is processed, if any one pixel of the plurality of pixels in the imaging array is defective.

[0009] According to another aspect of the invention, the video imaging system includes a second circuit, also formed in the substrate, that substitutes a corrected pixel for any pixel indicated as being defective by the first circuit. The corrected pixel may be generated by a histogramming circuit, a filter having a frequency response characteristic that approximates a modulation transfer function of the image formed on the imaging array, a median filter or an averaging filter.

[0010] According to yet another aspect of the invention, the video imaging system includes a gain control circuit, formed in the substrate, that adjusts the magnitude of the pixels in response to a gain control signal and the gain control signal is applied to the first circuit to control the analysis of the pixel to determine if it is defective.

Brief Description of the Drawings

[0011] Fig. 1 is a block diagram of a solid state imaging system in which the present invention; and

[0012] Fig. 2A is a partial front plan view of an imager array suitable for use with the present invention which shows several pixel elements.

[0013] Fig. 2B is a graph of amplitude versus distance that is useful for describing the point spread function of the illuminated pixel shown in Fig. 2A.

[0014] Fig. 3 is a block diagram of a x-y addressable imager having the detection and correction circuitry according to the present invention.

[0015] Fig. 4 is a block diagram of exemplary circuitry suitable for use as the defect detection circuitry shown in Fig. 3.

[0016] Fig. 5 is a block diagram of a portion of a first exemplary embodiment of circuitry suitable for use as the defect correction circuitry shown in Fig. 3.

[0017] Fig. 6A is a block diagram of a portion of a second exemplary embodiment of circuitry suitable for use as the defect correction circuitry shown in Fig. 3.

[0018] Fig. 6B is a pixel diagram that is useful for describing the operation of the circuits shown in Fig. 6A.

[0019] Fig. 7 is a block diagram of a second portion of the defect correction circuitry suitable for use with the embodiments shown in Figs. 5 and 6A.

[0020] Figs. 8A and 8B are block diagrams of alternate embodiments of circuitry suitable for use as the digital gain circuitry shown in Fig. 3.

[0021] Fig. 9 is a block diagram of gain-dependent threshold circuitry suitable for use with the defect detection circuitry shown in Fig. 3.

<u>Detailed Description of the Exemplary Embodiments</u>

[0022] Fig. 1, shows a solid state video imaging system 100 which incorporates an imager 116 and correction circuitry formed on a single substrate 112 according to the present invention. The substrate 112 is shown in a side-plan view. The imaging system 100 comprises imaging optics 110 which receives the light from the scene to be imaged and focuses the light the imager 116. The imaging system 100 also includes correction circuitry 118 which detects and corrects individual pixel errors in active video images produced by the imager array 116. In addition, the system 100 includes output circuitry 114 which processes the corrected image for display.

[0023] Imaging optics 110 may be composed of a combination of optical elements, which optical elements may include lenses, mirrors, lenticular arrays and/or aperture plates, by way of example. By a suitable choice of these optical elements, the numerical aperture, resolving power and spatial frequency filtering characteristics of imaging optics 110 may be selected. Due to the interaction of light with the optics 110 and the semiconductor surface, it is difficult to provide an optical system that illuminates only one pixel. Even if the optical system is designed to produce a very small spot on a single pixel, light from the spot may be diffused into adjacent pixels either by diffraction in the optics or by the

semiconductor material that is used to form the imaging device. Thus, the combined modulation transfer function of the optical system and the imager array typically spreads light across several pixels. The amount of light that is diffracted or diffused by the optics and/or semiconductor material may be small compared to the amount that is focused on the pixel but it is still more than is provided by a single defective pixel.

[0024] Another way of expressing the modulation transfer function is as a point-spread function. The point-spread function defines an area around a pixel in which signal can be detected. In a defective pixel, the signal is confined entirely within the pixel, resulting in a tightly-confined point-spread function. For an illuminated pixel, measurable signal may extend beyond the boundaries of the pixel resulting in a larger point-spread function.

[0025] This is especially true for back-illuminated imager arrays in which light or other types of radiation travels through the substrate before reaching the active pixel regions and for imager arrays that have field-free regions between the pixels. Defects such as white spots and black spots typically do not form in field-free regions. They only form in the field region of the pixel. Thus, for these two types of imager arrays, the point-spread function for an individual pixel is much tighter than the point-spread function of a spot of light focused on a single pixel of the imager. For front illuminated imager arrays and imager arrays that do not have field-free regions between the pixels, there is still a difference between the point-spread functions of the defective pixels and a single illuminated pixel but these differences may not be as large as for a back-illuminated imager or for an imager having field-free regions between the pixels.

[0026] In accordance with the principles of the present invention, the point-spread function of imager 116 is substantially higher than the point-spread function of a defective pixel so that single-pixel defects in the imager 116 may be distinguished from transitions in the image produced by the imaging optics 110.

[0027] Fig. 2A is a front-plan view of a portion of the imager array 116 which is useful for describing the difference in point-spread functions. Fig. 2 shows a plurality of pixel elements 210 and a minimum-size spot 212 produced by the imaging optics 110. As shown in Fig. 2A, although the minimum spot 212 is substantially confined to a single pixel, light energy, represented by the dashed-

line circle 214 can be detected by more than one pixel element 210 of the imager array 116.

[0028] The point-spread function of the spot 212 is shown in Fig. 2B. As shown in this Figure, the central area 212, corresponding to the active area of the pixel 210, is illuminated strongly but significant light energy 214 is spread among the adjacent pixels. The graph shown in Fig. 2B is not to scale but is exaggerated to illustrate the spread of light among adjacent pixels. As described above, this spread may be caused by the optics 110 or by diffraction and/or diffusion of light energy in the semiconductor material from which the imaging array is formed.

[0029] Also shown in Fig. 2A is a defective pixel 216. The signal from the defective pixel is substantially confined to the pixel 216 and is not seen as detectable energy in any of the adjacent pixels. Thus, a minimum-size feature of the focused image represents a more gradual transition among adjacent pixels than a defective pixel.

[0030] Referring to Fig. 3, the imaging system 100 comprises a substrate 112 of a semiconductor material, such as silicon. The imager array 116 and the correction circuitry 118 formed in the substrate as a single integrated circuit. In the exemplary embodiment of the invention, the imager array may be a CMOS imager such as is described in U.S. patent no. 5,920,345 to Sauer entitled CMOS IMAGE SENSOR WITH IMPROVED FILL FACTOR. Typical CMOS imagers generally include a plurality of pixels arranged in rows and columns. Each pixel generally includes an active region 210 (shown in Fig. 2) that receives light and converts the light to an electric charge. Each pixel 210 also generally includes a MOS transistor (not shown) which is used to amplify the accumulated charge from the pixel to an output port of the imager. A first set of conductors (not shown) extend between and parallel to the rows of the pixels and a second set of conductors (not shown) extend between and parallel to the columns of the pixels. This provides for x-y addressing of the pixels so that the electrons from the pixels may be provided to the output port one row at a time.

[0031] Also formed in the substrate 112 is the correction circuitry 118 including an analog to digital converter (ADC) circuit 312, which may be any of several well know types utilizing CMOS technology. An exemplary ADC is described in U.S. patent no. 5,272,481 entitled SUCCESSIVE

APPROXIMATION ANALOG TO DIGITAL CONVERTER EMPLOYING PLURAL FEEDBACK DIGITAL TO ANALOG CONVERTERS. The imager array 116 provides an analog video signal, AV, to the ADC 312. The ADC 312 digitizes the signal AV to provide an uncorrected video signal, UV. The signal UV is applied to digital gain circuitry 314 and, in the exemplary embodiment of the invention, as an output signal of the imaging system 100. The gain circuitry 314 is also formed in the substrate 112 as a CMOS circuit. The exemplary gain circuit 314 receives an external gain signal, GAIN, which determines the amount of amplification or attenuation that is applied to the signal UV to generate the gain-adjusted video signal PIN. Exemplary digital gain circuitry is described below with reference to Figs. 8A and 8B.

[0032] Fig. 8A includes a digital multiplier 810 which simply multiplies the uncorrected video signal UV by the signal GAIN. Fig. 8B replaces the digital multiplier by a look-up table (LUT) 812, which is addressed by the values of the pixel signal UV and the signal GAIN to effectively multiply the signals UV and GAIN. For certain types of signals it may be desirable to use the LUT 812 rather than the digital multiplier 810 because a wider range of gain functions may be implemented using the LUT than are possible using the multiplier (e.g. the gain function may be non-linear to perform contrast enhancement or to implement gamma correction).

[0033] The digital gain circuitry 314 applies the signals PIN and GAIN to the defect detection circuitry 316 and applies the signal PIN to the defect substitution circuitry 318. As described below, the defect detection circuitry 316 identifies defective pixel values from the gain-adjusted pixel signal PIN provided by the digital gain circuitry 314 and provides a signal DEF indicating that a defective pixel has been identified. The defect substitution circuitry 138 calculates a substitute pixel value for the current pixel value being provided by the system 100 and provides either the signal PIN or the substitute pixel value responsive to the signal DEF.

[0034] In the operation of the video imaging system 100, the scene image is projected on the x-y imager 116 through the optics 110 (all shown in Fig. 1). As described above, the image of a point source projected onto the imager 116 has energy which encompasses multiple neighboring pixels. The real time pixel rate signal is analyzed by the on-chip circuits which make the determination based on

modulation transfer function (MTF) or point spread, if a white or black pixel is defective or due to scene content. The defect detector 38 separates scene content from defective pixel induced signal by real time comparison of a pixel with its neighbors. A pixel memory, and optionally one or more line memories, may be used for this comparison.

[0035] Exemplary defect detection circuitry 316 is shown in Fig. 4. The exemplary circuitry 316 includes a filter 410 and hysteresis circuitry 411 which compares a pixel value Po with the output signal provided by the filter to determine if the Po represents an erroneous value. In the exemplary embodiment of the invention, the filter 410 is a finite impulse response (FIR) filter that receives the gain-adjusted pixel signal PIN and provides an output signal PFILT. The exemplary filter includes four one-pixel period delay stages, 412, 414, 416 and 418 which provide four or five pixel values to four or five multipliers, 422, 424, 428, 430 and, optionally 426. The signal Po is the pixel signal provided by the delay element 414. In the exemplary embodiment of the invention, the signal Po may or may not contribute to the filtered pixel value, as indicated by the "x" on the input to the multiplier 426, shown in phantom. This prevents the pixel Po from distorting the filtered value when Po is defective.

[0036] These pixel values are five successive pixel values on a single line of the video signal. Each of the five multipliers is coupled to receive a respective coefficient value 432, 434, 438, 440 and, optionally 426. The output signals of the multipliers 422, 424, 428, 430 and, optionally, 426 are summed by a summing circuit 442 to produce the output value PFILT. In the exemplary filter shown in Fig. 4, the coefficients provide the filter with a frequency response characteristic that approximates the spatial frequency response characteristic (i.e. the modulation transfer function) of the optics 110. The exact values of the coefficients depend on the frequency response characteristic of the optics 110 and can be readily determined by one of ordinary skill in the art. It is contemplated that the filter 410 may be implemented to have a different frequency response characteristic. For example, each of the five coefficient values 432, 434, 436, 438 and 440 may be 0.2, so that the output signal provided by the filter is the arithmetic average of the five successive pixel values. Alternatively, the filter 410 may include a median filter (not shown) such that the signal PFILT is the median of the signal PIN and the signals provided by the delay elements 412, 416, 418 and, optionally, 414.

[0037] The exemplary hysteresis circuitry 411 includes a multiplier 444, that multiplies the signal PFILT, provided by the filter 410, by a threshold value 446 to generate a signal δ which is added to PFILT in an adder 448 and subtracted from PFILT in subtracter 450 to generate boundary signals. The boundary signals are compared to Po in the two comparators 452 and 454. If Po is greater than PFILT+δ or less than PFILT-δ then the pixel may represent an error. In the exemplary hysteresis circuitry 411, the output signals of the comparators 452 and 454 are applied to an OR gate 460 to generate the output signal DEF of the defect detection circuitry 316. In an alternative embodiment of the invention, the value of the threshold 466 changes as a function of the signal GAIN, representing the amount of amplification or attenuation that is applied to the signal UV by the digital gain circuitry 314. In this alternative embodiment, the threshold circuit 446 may have the structure shown in Fig. 9.

[0038] The threshold circuit shown in Fig. 9 includes a digital decoder 910 that is coupled to receive the signal GAIN. The circuit 446 also includes a plurality of threshold values, for example, 912, 914, 916 and 918, and a multiplexer 920. The decoder 910 decodes the signal GAIN to select one of the threshold values 912, 914, 916 and 918 to apply to the multiplier 444 (shown in Fig. 4). The threshold value applied when the gain is relatively large is greater than the threshold value applied when the gain is relatively low. The decoder 910 divides the range of values for the signal GAIN into four sub-ranges, each corresponding to a respectively different threshold value. It is contemplated that the sub-ranges may represent a linear division of the range of the signal GAIN or some other division, for example a logarithmic division. It is also contemplated that the threshold values may increase linearly or by some other function, for example, exponentially.

[0039] The hysteresis circuitry 411 inhibits correction of defective pixels when the difference between the defective pixel value Po and the pixel value PFILT is less than the threshold value. For example, a black pixel in a dark area of the image is not corrected nor is a white pixel in a bright area of the image. Leaving these pixels uncorrected prevents loss of information that may be represented by the defective pixel.

[0040] Although the exemplary circuitry shown in Fig. 4 is a digital, it is contemplated that equivalent circuitry may be made using analog circuitry. In this

alternative embodiment, the delay elements 412, 414, 416 and 418 may be implemented as sample-and-hold circuits (not shown). The multipliers 422, 424, 426, 428 and 430 may be implemented as amplifiers (not shown) where each amplifier is configured to have a gain corresponding to a respective one of the coefficients 432, 434, 436, 438 and 440. The summing circuit 422 may be a resistive summing network (not shown) as may the adder 448. The multiplier 444 may be a variable-gain amplifier (not shown) which receives an analog threshold signal at its gain input. The subtracter 450 may be replaced by a unity-gain differential amplifier (not shown). In an analog implementation of the defect detect detection circuitry, the gain control circuitry 314 may be implemented as a conventional analog automatic gain control (AGC) device, in which the gain signal is provided to the defect detection circuitry 316 as the threshold signal. Furthermore, in an analog implementation, the analog signal PFILT may be used as the substitute pixel value.

[0041] After a pixel is determined to be defective, it is corrected by value substitution derived from neighboring nondefective pixels. This can be accomplished using know techniques such as averaging the value of signal from all neighboring pixels and substituting this derived value in place of the defective pixel. This value to be substituted may be generated by other means, such as using the median of the surrounding pixel values or generating a histogram of the surrounding pixels and substituting the pixel value having the greater frequency of occurrence for the defective pixel. Alternatively, the substituted pixel value may be interpolated from any two or more of the neighboring pixel values. The neighboring pixels used by the defect detector and the defect substitution circuitry may not be the same. Either of these devices may use the immediately surrounding pixels or pixels extending for a predetermined number of pixel positions (e.g., 2-8) from the target pixel.

[0042] The exemplary defect substitution circuitry 318 described below includes two parts. The first part generates a corrected pixel value and a corresponding un-corrected value while the second part selects between the corrected and uncorrected values responsive to the defect signal DEF, provided by the defect detection circuitry 316, described above. In the described exemplary embodiments, the second part of the defect substitution circuitry is the same, and is shown in Fig. 7. Two different options are shown for the first part: a histogram circuit, shown in Fig. 5 and a filtering circuit, shown in Figs. 6A and 6B.

[0043] Fig. 5 shows a histogram circuit that may be used to generate a substitute pixel value. The histogram circuit is similar to that described in U.S. patent to McCaffrey except that the image is divided into a plurality of regions and separate histogram statistics are maintained for each region of the image. As shown in Fig. 5, the exemplary histogram circuit includes a histogram generator 510 and a section memory 512. Both of these devices are coupled to receive address signals from an address counter 514. At any given time, the address signal is the address of the pixel value PIN currently being applied to the histogram generator 510. The exemplary histogram generator 510 monitors pixel values in each of the defined regions of the image, responsive to the address values provided by the address generator, and stores statistics on the frequency of occurrence of each value in the section memory 512. The output signal PF of the section memory 512 is the most frequently occurring value for the current section.

[0044] The exemplary histogram circuit shown in Fig. 5 assumes that the image data in the current field or frame is roughly the same as the image data in the previous field or frame because, when a new image is processed, the image data stored in the section memory 512 is from the previous image field or frame. Consequently, this circuit may cause erroneous pixel values to be produced for rapidly moving objects or immediately after scene changes. For most image data, defects of this type are acceptable because they are of short duration and are typically masked by the movement in the image or the scene change. It is contemplated that these defects may be eliminated by delaying the signal PIN by one field or frame time, in parallel with the histogram generating circuitry, so that the statistics accumulated in the section memory 512 match the output signal PIN.

[0045] Another exemplary circuit for generating substitute pixel values is shown in Figs. 6A and 6B. Fig. 6A shows an exemplary circuit while Fig. 6B is a pixel layout which shows the relative positions in an image of the pixels that are to be filtered. With reference to Fig. 6B, the circuit shown in Fig. 6A generates a substitute pixel value for a target pixel 638 by filtering the surrounding pixel values 632, 634 and 640. It is contemplated that the target pixel value 638 may or may not be included among the filtered pixel values. The target pixel 638 and its surrounding pixels are provided by the cascade connected delay elements 610, 612, 614, 616, 618, 620, 622 and 624, shown in Fig. 6A. The pixels 632 shown in Fig. 6B are provided by the delay elements 624, 622 and 620. The pixels 636, 638 and 640 are provided by the delay elements 618, 616 and 614 while the pixels

634 are provided by the delay elements 612 and 610 with the right-most pixel 634 being the input pixel PIN. Each of the delay elements 610, 612, 616, 618, 622 and 624 is a one pixel period delay. Delay elements 614 and 620 each provides a delay of one horizontal line interval minus two pixel periods.

[0046] The pixel value PIN and the pixel values provided by the delay elements 610, 612, 614, 616, 618, 620, 622 and 624 are applied to a filter 626. The filter 626 used in the exemplary embodiment of the invention may be a simple averaging filter, a median filter, an interpolation filter or a low-pass filter. If the filter 426 is a low-pass filter, it may have a frequency response characteristic corresponding to the spatial frequency spectrum of the optics 110, shown in Fig. 1. As shown by the "x" on the filter input line from the delay element 616, it is contemplated that the target pixel value 638 may or may not be included among the filtered pixel values. The output signal of the filter is a signal PF' which is the substitute pixel value. The filter also provides the signal PIN, delayed by one horizontal line time plus one pixel period (i.e. the pixel 638) as an output signal PIN'. This pixel value is the unmodified pixel value that corresponds in position in the image to the pixel value provided by the filter 626.

[0047] As an alternative to using the filter shown in Fig. 6A, the substitute pixel value may be the pixel value PFILT provided by the exemplary defect detection circuitry 316, shown in Fig. 4. In this instance, the unmodified pixel value may be the pixel Po provided by the delay element 414, also shown in Fig. 4.

[0048] Fig. 7 shows the circuitry which may be used with the circuitry shown in Figs. 5 or 6A or with the signals PFILT and Po generated by the circuitry shown in Fig. 4 to provide the output signal, OUT, of the imaging system 100, as shown in Fig. 3. The combination of the circuitry shown in Fig. 5 or 6A and the circuitry shown in Fig. 7 produces the defect substitution circuit 316, shown in Fig. 3. Alternatively, if the signals PFILT and Po from the defect detection circuitry 316 are used as the modified and unmodified pixel values, as shown in phantom in Fig. 3, the circuitry shown in Fig. 7 may constitute the defect substitution circuitry 318. In this instance, the signal PIN would not be needed by the defect substitution circuitry 318, as indicated by the "x" in Fig. 3.

[0049] The circuitry shown in Fig. 7 includes two optional compensating delay elements 710 and 712 and a multiplexer 714. The delay element 710 is coupled to receive a modified pixel signal (e.g. PF, PF' or PFILT) while the delay element 712 is coupled to receive the corresponding unmodified pixel value (e.g. PIN, PIN' or Po). The delay elements 710 and 712 compensate for any difference in processing delay between the defect detection circuitry 316 and the defect substitution circuitry 318. These delay elements ensure that the signal DEF provided by the defect detection circuitry 316 to the control input terminal of the multiplexer 714 corresponds to the pixel position of the pixel signals provided to the two signal input ports of the multiplexer. While the compensating delay elements are shown as being applied to the defect substitution circuitry 318, it is contemplated that a single compensating delay element (not shown) may be used, instead, to provide the signal PIN to the defect detection circuitry when the processing delay through the defect substitution circuitry 318 is greater than the delay through the defect detection circuitry 316.

[0050] When the signal DEF indicates that the defect detection circuitry has detected a defective pixel, the multiplexer 714 passes the modified pixel value (e.g. PF, PF' or PFILT). When no defect is indicated, the multiplexer 714 passes the unmodified pixel value (e.g. PIN, PIN' or Po).

[0051] Thus there is provided by the present invention a video imaging system having real time on-chip detection and correction which is controlled by the gain applied to the detected video signal. This system requires no user intervention and can significantly reduce the cost of CMOS image sensors through increased yield of usable imager arrays. The imager array appears defect free as soon as it is turned on. Because the pixel defect detection is performed in real time and does not depend on data stored in memory, the decision whether or not to correct a pixel is made for each pixel once per frame. This allows defect detection threshold to be based on factors, such as scene brightness and imager temperature. The imager self corrects pixels as required. Because the circuitry corrects pixels based only on their current state and the current state of the surrounding pixels, the circuitry may be used to correct transient errors such as those generated by gamma rays.

[0052] When the defect detection circuit 316 is implemented using analog circuitry, the defect substitution circuitry 318 may include an analog multiplexer

(not shown) formed, for example by two three-state circuits having a common output terminal. One of the three-state circuits may be coupled to receive the signal Po, provided by the sample-and-hold circuit 414 while the other circuit is coupled to receive the signal PFILT provided by the summing junction 442. In this implementation, the circuit for the signal that is not selected would be held in a high-impedance state.

[0053] While the invention has been described in terms of an exemplary embodiment, it is contemplated that it may be practiced as described above with variations within the scope of the appended claims.